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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,938	10/15/2003	Yee-Chia Yeo	TSM03-0926	7692

43859 7590 10/04/2006

SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,938	YEO ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/15/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 7, 9, 10, 13, 15, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al., hereinafter Yamaguchi (US Patent Application Publication 2002/0048972), previously cited.

Regarding claims 1, 2, 9, 10, and 13, Yamaguchi discloses in figure 8C, a semiconductor chip comprising:

a SOI substrate 10 comprising an active region (the region immediately surrounding region 36);

a first transistor structure 20 formed in/on the active region, the first structure is fully silicided by the silicide 38, and having source and drain (see paragraph 72);

and

at least one dummy silicide structure 22 formed on the substrate.

Regarding claims 4 and 15, the dummy silicide region is located in the active region, as can be seen in the figure.

Regarding claims 5 and 16, the dummy structure is located in an isolation region 16 separate from the active region.

Regarding claims 7 and 18, silicide 38 is titanium silicide (see paragraph 61).

3. Claims 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Koubuchi et al., hereinafter Koubuchi (US Patent 6,261,883), previously cited.

Koubuchi discloses in figure 16, a substrate 1 comprising an active region;

A first silicided structure 7a; and a dummy silicided structure 34a is formed on the semiconductor substrate. Also, an etch stop/dielectric layer 8c, which can be silicon nitride, see col. 20, line 40, is overlying the first structure and the dummy structure. See the specification, wherein on page 17 it is indicated that the etch stop layer can be silicon nitride.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi.

Yamaguchi discloses the limitation in the claim, as discussed above, except for expressly disclosing electrical contacts are coupled to the gate, source and drain regions. It would have been obvious to one of ordinary skill in the art at the time of the invention to supply electrical contacts to those regions to make the transistor usable in an application.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Yamaguchi reference as applied to claim 2 above, and further in view of Yu (US Patent 6,686,248), previously cited.

The Yamaguchi reference discloses the claimed invention, as discussed above, except for a gate dielectric comprising a high permittivity dielectric selected from the group consisting of aluminum oxide, hafnium oxide and such.

Yu discloses that these materials are used as high dielectric constant material of a gate dielectric. Therefore, it would have been obvious to one of ordinary in the art at the time of the invention to use these materials as the gate dielectric of the Yamaguchi reference to be able to use the transistor in an application, which requires a gate with high dielectric constant. See *In re Leshin*, 125 USPQ 416, for the proposition that it is within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

7. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yamaguchi reference as applied to claim 1 above, and further in view of Paton et al., hereinafter Paton (US Patent 6,873,051), previously cited.

The Yamaguchi reference discloses the claimed invention, as discussed above, except for the dummy silicide structure is nickel silicide.

Paton discloses nickel silicide in a gate silicide structure offers advantages such as low temperature formation (see column 1, lines 45-48). Therefore, it would have been obvious to one of ordinary in the art at the time of the invention to use Nickel silicide as the silicide layer of the Yamaguchi reference since the advantages of using Nickel as a gate silicide were known in the art. See *In re Leshin*, 125 USPQ 416, for the proposition that it is within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

8. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yamaguchi reference, as applied to claim 1 above, and further in view of Holmes et al., hereinafter Holmes (US Patent 6,797,641), previously cited.

The Yamaguchi reference discloses the claimed invention, as discussed above, except for the dummy silicide structure comprises germanium.

Holmes discloses a gate structure comprises germanium silicide (see column 2, lines 14-22), further disclosing this gate structure improves reliability of the gate structure (see column 1). Therefore, it would have been obvious to one of ordinary in the art at the time of the invention to use germanium in the structure of the gates of the Yamaguchi reference to improve the reliability of the structure therein. See *In re Leshin*, 125 USPQ 416, for the proposition that it is within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Response to Arguments

9. Applicants' arguments filed on 7/18/06 have been fully considered but they are not persuasive for the following reasons.

First, there is not a clear definition of the phrase "dummy...structure" in the specification. Therefore, the dummy gate of the Yamaguchi reference, which is properly is called as such, qualifies as a dummy structure.

Assuming, arguendo, that the dummy gate should read on a gate that does not perform a logic function, which has been given as an example of a dummy gate (see paragraph 32 of the specification) and is not a clear and deliberate definition of a dummy gate, the phrase "logical

function" is too broad and vague for one of ordinary skill in the art to determine as to what exactly qualifies as a dummy gate. As far as can be determined, the dummy gate of the Yamaguchi reference does not perform a "logical function" since it has merely a parasitic capacitance, as mentioned in several occasions in the reference. An element being a parasitic capacitance does not mean that element performs a logical function. Logical function is normally associated with logic gates, or at most to other logic blocks in digital integrated circuits.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DF

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER